In paragraph 4, the Examiner rejected claims 15-17, 19, 21-23, 25-30, 32-35, 37, 39, 41-46, and 48-49 under 35 U.S.C. 102(e) as being anticipated by Nagata. In paragraph 6, the Examiner rejected claims 18 and 36 under 35 U.S.C. 103(a) as being unpatentable over Nagata in view of Platt. In paragraph 7, the Examiner rejected claims 20 and 38 under 35 U.S.C. 103(a) as being unpatentable over Nagata in view of Gerzon. On page 9, the Examiner rejected claims 24 and 40 under 35 U.S.C. 103(a) as being unpatentable over Nagata in view of Myers. In paragraph 8, the Examiner rejected claims 31 and 47 under 35 U.S.C. 103(a) as being unpatentable over Nagata in view of Platt, Gerzon, and Myers. For the following reasons, the Applicant submits that all of the pending claims are allowable over the cited references.

Claim 15 is directed to apparatus for generating a delayed output digital audio signal from an input digital audio signal. The apparatus comprises a first delay module and a second delay module. The first delay module applies a first amount of delay to the input digital audio signal to generate a partially delayed digital audio signal, where the first delay module selects the first amount of delay from a plurality of available first delay values separated from one another by increments at a first resolution level. The second delay module applies a second amount of delay to the partially delayed digital audio signal to generate the delayed output digital audio signal, where the second delay module selects the second amount of delay from a plurality of available second delay values separated from one another by increments at a second resolution level different from the first resolution level. The Applicant submits that the cited references do not teach or even suggest such a combination of features.

In rejecting claim 15, the Examiner cited delay units 61 and 71 shown in Fig. 2 of Nagata as being examples of the first and second delay modules of claim 15. In particular, the Examiner suggested that "by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50," there is "a chance" that the resolution of the delay increments of delay unit 71 will be different from the resolution of the delay increments of delay unit 61, citing column 4, line 60, to column 5, line 67, of Nagata. The Applicant submits that this constitutes a misinterpretation of the teachings in Nagata. In particular, the Applicant submits that there are no teachings or even suggestions in Nagata to support a conclusion that the resolution of the delay increments of delay unit 71 is ever different from the resolution of the delay increments of delay unit 61.

Nagata discloses in Fig. 2 an echo effector having a preceding stage connected to a succeeding stage and a microcomputer 65 for controlling both stages. See column 4, lines 42-448. As shown in Fig. 2, the output signal from the preceding stage (i.e., the output from adder 15) is applied directly to the input of the succeeding stage, where a copy of that signal is applied directly to delay unit 71.

According to Nagata, a digital audio input signal is applied to input terminal 20 of the preceding stage, where one copy of that signal is applied to adder 14 and another copy is applied to adder 15. See column 4, line 48-51. The output from adder 14 is applied directly to delay unit 61. See column 4, line 52-53. Delay unit 61 is a memory device that "operates according to an address counted in synchronization with a sampling clock for sequentially writing data of the signal to be delayed into the memory, and for sequentially reading out the data after a given time interval, thereby achieving the signal delay." See column 4, lines 53-59. In other words, the delay increment for delay unit 61 (i.e., the time interval between successive delay values that can be provided by delay unit 61) is directly related to the sampling rate of the digital audio input signal applied to input terminal 20.

Nagata also teaches that delay unit 71 is also a memory device (e.g., a RAM) that "operates according to an address counted in synchronization with a sampling clock for sequentially writing data of the preceding output signal to be delayed into the RAM and for successively reading the data after a

given time interval, thereby achieving the signal delay in a manner similar to the preceding delay unit 61." See column 5, lines 14-21.

Since Nagata discloses in Fig. 2 that (1) copies of the digital audio input signal at input terminal 20 are applied directly to both adder 14 and adder 15, (2) the digital audio output signal from adder 14 is applied directly to delay unit 61, and (3) a copy of the digital audio output signal from adder 15 is applied directly to delay unit 71, the Applicant submits that the Nagata implicitly teaches that the sampling rate of the data stored in delay unit 61 is identical to the sampling rate of the data stored in delay unit 71. Since the delay increments of both delay unit 61 and delay unit 71 are directly related to the data sampling rate, the Applicant submits that the delay increment of delay unit 61 is identical to the delay increment of delay unit 71.

Notwithstanding the Examiner's statement otherwise, the Applicant submits that "adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50" does not change the delay increment of either delay unit 61 or delay unit 71. According to explicit teachings in Nagata, "the state of the switch matrix 45, the dials 41, 48 and 49, and the command switch 50" is used by microcomputer 65 to retrieve control data from memory 66 in order to calculate the gain factors GF, GD1-GD*n*, GL1-GL*n*, and GR1-GR*n* and to select the delay terminals TF, TD1-TD*n*, TL1-TL*n*, and TR1-TR*n*. See column 5, lines 39-44, and column 6, lines 14-20.

The gain factors GF, GD1-GD*n*, GL1-GL*n*, and GR1-GR*n* correspond to the gains applied by the various multipliers 64, 621-62*n*, 73L1-73L*n*, and 73R1-73R*n*. Changing these gain factors has no affect on the delay increment of either delay unit 61 or delay unit 71.

The different delay terminals TF, TD1-TD*n*, TL1-TL*n*, and TR1-TR*n* correspond to different delay values that are available by delay units 61 and 71. Changing the selection of the delay terminals changes the delay values that are applied to the digital audio signals, but it does not change the delay increment of either delay unit 61 or delay unit 71.

Nagata does teach that the delay range provided by delay unit 71 can be changed (using dial 48 and command switch 50). See column 7, lines 1-27. Significantly, however, such a change in the delay range does not change the delay increment. In the example shown in Fig. 4, the delay range is changed from the old range of 100-200 msec to a new range of 115-215 msec. Significantly, the delay increment (i.e., the delay interval between successive available delay values) for the new range is exactly the same as the delay increment for the old range (i.e., 5 msec).

Thus, while it is true that Nagata teaches the ability to change the delay values provided by delay units 61 and 71 and the ability to change the delay range provided by delay unit 71, Nagata does not teach or even suggest the ability to change the delay increment of either delay unit 61 and delay unit 71.

In view of the foregoing, the Applicant submits that Nagata teaches only that the delay increment of delay unit 61 is identical to the delay increment of delay unit 71. As such, Nagata does not teach or even suggest first and second delay modules, where the resolution level of the delay increments of the second delay module is different from the resolution level of the delay increments of the first delay module.

The other cited references fail to provide the features of claim 15 that are missing from Nagata.

For all these reasons, the Applicant submits that new claim 15 is allowable over the cited references. For similar reasons, the Applicant submits that new claims 33 and 49 are allowable over the

cited references. Since the rest of the claims depend variously from claims 15 and 33, it is further submitted that those claims are also allowable over the cited references.

In view of the above remarks, the Applicant believes that the pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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